EXHIBIT B

UNITED STATES DISTRICT COURT

DISTRICT OF GUAM

NANYA TECHNOLOGY CORP. and NANYA TECHNOLOGY CORP. U.S.A., *Plaintiffs,* v. FUJITSU LIMITED and FUJITSU MICROELECTRONICS AMERICA, INC., *Defendants.*	Case No. CV-06-00025 **DECLARATION OF KIMBERLY WILSON**

I, Kimberly Wilson, hereby declare as follows:

1. My name is Kimberly Wilson and I am a travel agent with Canyon Creek Travel. I am over the age of 21 and am competent to make this declaration. All of the statements set forth herein are true and correct and are based on my professional practice and personal knowledge. The flight times and availability of flights are subject to change based upon daily and periodic fluctuations.

2. The flight time between Tokyo, Japan to Tamuning, Guam is approximately three to four hours. The geographic distance between Tokyo, Japan and Tamuning, Guam is approximately 1561 miles. The time difference between Tokyo, Japan and Tamuning, Guam is one hour.

3. Based upon figures published by the Guam Visitors Bureau, in 2006, of the approximately 1.2 million visitors to Guam, approximately 79% came from Japan. The second largest number of visitors to Guam came from Korea with approximately 9%. There are nine cities in Japan with direct flights to Guam. In contrast, there are only three cities in Japan with direct flights to San Francisco, California.

3. The flight time between Tokyo, Japan to San Francisco, California is approximately nine to ten hours. The geographic distance between Tokyo, Japan and San Francisco, California is approximately 5131 miles. The time difference between Tokyo, Japan and San Francisco, California is sixteen hours. Thus, the distance between Tokyo, Japan and San Francisco, California is over three times as far as between Tokyo, Japan and Tamuning, Guam and it takes approximately three times as long to get from Tokyo to San Francisco as it takes to get from Tokyo to Guam.

4. The flight time between Taipei, Taiwan and Tamuning, Guam is approximately three to four hours. The geographic distance between Taipei, Taiwan and Tamuning, Guam is approximately 1721 miles. The time difference between Taipei, Taiwan and Tamuning, Guam is two hours.

5. The flight time between Taipei, Taiwan and San Francisco, California is approximately eleven to twelve hours. The geographic distance between Taipei, Taiwan and San Francisco, California is approximately 6450 miles. The time difference between Taipei, Taiwan and San Francisco, California is fifteen hours. Thus, the distance between Taipei, Taiwan and San Francisco, California is almost four times as far as between Taipei, Taiwan and Tamuning, Guam and it takes approximately three times as long to get from Taipei to San Francisco as it takes to get from Taipei to Guam.

6. Additionally, the geographic distance between San Francisco International Airport and the federal courthouse in Oakland is approximately 22 miles and takes approximately 40 minutes to travel. The geographic distance between the Guam airport and the federal courthouse for the District of Guam is approximately less than five miles and takes approximately 10 minutes to travel. Thus, overall, the total travel time from Tokyo to the federal

courthouse in Oakland is over three times longer than it is from Tokyo to the federal courthouse in Guam. Also, the overall, the total travel time from Taipei to the federal courthouse in Oakland is approximately four times longer than it is from Taipei to the federal courthouse in Guam.

I DECLARE UNDER PENALTY OF PERJURY UNDER THE LAWS OF THE UNITED STATES OF AMERICA THAT THE FOREGOING IS TRUE AND CORRECT.

SIGNED ON THE 2 DAY OF MAY, 2007

SIGNATURE Kimberly Wilson

PRINTED NAME Kimberly Wilson

TITLE Agent - Canyon Creek Area

EXHIBIT C

UNITED STATES DISTRICT COURT
DISTRICT OF GUAM

NANYA TECHNOLOGY CORP. and NANYA TECHNOLOGY CORP. U.S.A., *Plaintiffs,* v. FUJITSU LIMITED and FUJITSU MICROELECTRONICS AMERICA, INC., *Defendants.*	Case No. CV-06-00025 **DECLARATION IN SUPPORT OF PLAINTIFFS' RESPONSE TO DEFENDANTS' MOTION TO IMMEDIATELY TRANSFER FOR CONVENIENCE**

1. Nanya Technology Corporation ("NTC") is a Taiwanese corporation having its principal place of business in Hwa Ya Technology Park, 669, Fu Hsing 3rd Rd., Kueishan, Taoyuan, Taiwan, Republic of China.

2. Nanya Technology Corporation U.S.A. ("NTC USA") is a wholly owned subsidiary of NTC. NTC USA is NTC's sales office for America. NTC USA's employees do not conduct any relevant research and/or production of the patents-in-suit or accused devices.

3. Several of NTC U.S. Patents are at issue in this matter, including U.S Patent No. 6,225,187 ("the '187 Patent"); U.S. Patent No. 6,426,271 ("the '271 Patent"); and U.S. Patent No. 6,790,765 ("the '765 Patent").

4. Tse-Yao Huang, Yun-Sen Lai, Yi-Nan Chen, Hsien-Wen Liu, and Hui-Min Mao, inventors of the '187, '271, and '765 Patents all reside in Taiwan. All documents related to the original design and manufacturing of the invention described in the '187, '271, and '765 Patents, including inventor's notes, product specifications, conception, and reduction to practice (to the extent such documents exist), are located in Taiwan.

5. Defendants have accused NTC and NTC's semiconductor memory products of infringing certain Fujitsu Ltd. U.S. Patents. The majority of documents related to the original design and manufacturing of NTC's semiconductor memory products, including engineer's notes

and production specifications, are located in Taiwan. The majority of documents related to NTC's sales, offers to sell, use, importation, exportation, and distribution of its semiconductor memory products are located in Taiwan. The majority of engineers and persons with knowledge of NTC's semiconductor memory products reside in Taiwan.

6. Representatives from NTC and Fujitsu Ltd. participated in license negotiations from 1999 to 2005 with respect to the Fujitsu Ltd. U.S. patents-in-suit, all of which occurred in either Taiwan or Japan. All representatives from NTC who participated in these license negotiations reside in Taiwan.

7. NTC is relatively small compared to Fujitsu Ltd. NTC's engineers and other NTC personnel with knowledge of relevant facts have limited available time to travel for depositions, hearings, trial, and other proceedings. A venue closer to Taiwan would permit NTC personnel to more efficiently and easily participate in such proceedings. Air travel from Taiwan to Guam takes about three hours compared to eleven hours to California and does not require crossing the International Date Line. Conducting this lawsuit in Guam compared to California would permit NTC personnel to return to work after participating in such proceedings with substantially less delay and expense.

I DECLARE UNDER PENALTY OF PERJURY UNDER THE LAWS OF THE UNITED STATES OF AMERICA THAT THE FOREGOING IS TRUE AND CORRECT.

SIGNED ON THE 2nd DAY OF MAY, 2007.

SIGNATURE _____

PRINTED NAME Hong-chi Chang

TITLE Deputy Director, Marketing DIV.

EXHIBIT D

UNITED STATES DISTRICT COURT

DISTRICT OF GUAM

NANYA TECHNOLOGY CORP. and NANYA TECHNOLOGY CORP. U.S.A., *Plaintiffs,* v. FUJITSU LIMITED and FUJITSU MICROELECTRONICS AMERICA, INC., *Defendants.*	Case No. CV-06-00025 **DECLARATION OF ASHLEY NICOLE MOORE**

I, ASHLEY NICOLE MOORE, DECLARE UNDER PENALTY OF PERJURY THAT THE FOLLOWING IS TRUE AND CORRECT:

1. I am registered to practice before the United States Patent and Trademark Office. It is my understanding that the patents-in-suit include the following: U.S. Patent No. 4,384,918, U.S. Patent No. 4,458,336, U.S. Patent No. 4,527,070, U.S. Patent No. 4,539,068, U.S. Patent No. 4,641,166, U.S. Patent No. 4,692,689, U.S. Patent No. 4,801,989, U.S. Patent No. 5,227,996, U.S. Patent No. 5,339,273, U.S. Patent No. 5,397,432, U.S. Patent No. 5,688,712, U.S. Patent No. 5,841,731, U.S. Patent No. 6,104,486, U.S. Patent No. 6,292,428, and U.S. Patent No. 6,320,819.

2. U.S. Patent No. 4,384,918 identifies Naomichi Abe as the sole inventor and Fujitsu Limited as the assignee. Naomichi Abe is identified as residing in Tokyo, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 4,384,918's front page, which bears this information, is attached hereto as Exhibit A.

3. U.S. Patent No. 4,458,336 identifies Yoshihiro Takemae as the sole inventor and Fujitsu Limited as the assignee. Yoshihiro Takemae is identified as residing in Yokohama, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No.

4,458,336's front page, which bears this information, is attached hereto as Exhibit B. Also attached as Exhibit C is a declaration signed by Yoshihiro Takemae confirming under penalty of perjury the inventor's residence in Japan.

4. U.S. Patent No. 4,527,070 identifies Shougo Matsui, Yoshimitu Mashima, and Kenichi Kobayashi as the inventors and Fujitsu Limited as the assignee. Shougo Matsui is identified as residing in Sagamihara, Japan, Yoshimitu Mashima is identified as residing in Kawasaki, Japan, Kenichi Kobayashi is identified as residing in Tokyo, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 4,527,070's front page, which bears this information, is attached hereto as Exhibit D. Also attached as Exhibit E is a declaration signed by Shougo Matsui, Yoshimitu Mashima, and Kenichi Kobayashi confirming under penalty of perjury each inventor's residence in Japan.

5. U.S. Patent No. 4,539,068 identifies Mikio Takagi, Kanetake Takasaki, and Kenji Koyama as the inventors and Fujitsu Limited as the assignee. Mikio Takagi is identified as residing in Kawasaki, Japan, Kanetake Takasaki is identified as residing in Tokyo, Japan, Kenji Koyama is identified as residing in Yokosuka, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 4,539,068's front page, which bears this information, is attached hereto as Exhibit F. Also attached as Exhibit G is a declaration signed by Mikio Takagi, Kanetake Takasaki, and Kenji Koyama confirming under penalty of perjury each inventor's residence in Japan.

6. U.S. Patent No. 4,641,166 identifies Yoshihiro Takemae, Tomio Nakano, and Kimiaki Sato as the inventors and Fujitsu Limited as the assignee. Yoshihiro Takemae is identified as residing in Tokyo, Japan, Tomio Nakano is identified as residing in Kawasaki, Japan, Kimiaki Sato is identified as residing in Tokyo, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 4,641,166's front page, which bears this information, is attached

hereto as Exhibit H. Also attached as Exhibit I is a declaration signed by Yoshihiro Takemae, Tomio Nakano, and Kimiaki Sato confirming under penalty of perjury each inventor's residence in Japan.

7. U.S. Patent No. 4,692,689 identifies Yoshihiro Takemae as the sole inventor and Fujitsu Limited as the assignee. Yoshihiro Takemae is identified as residing in Tokyo, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 4,692,689's front page, which bears this information, is attached hereto as Exhibit J.

8. U.S. Patent No. 4,801,989 identifies Masao Taguchi as the sole inventor and Fujitsu Limited as the assignee. Masao Taguchi is identified as residing in Sagamihara, Japan, and Fujitsu Limited is identified as residing in Kanagawa, Japan. A true and correct copy of U.S. Patent No. 4,801,989's front page, which bears this information, is attached hereto as Exhibit K. Also attached as Exhibit L is a declaration signed by Masao Taguchi confirming under penalty of perjury the inventor's residence in Japan.

9. U.S. Patent No. 5,227,996 identifies Toshiya Uchida as the sole inventor and Fujitsu Limited as the assignee. Toshiya Uchida is identified as residing in Kawasaki, Japan, and Fujitsu Limited is identified as residing in Kanagawa, Japan. A true and correct copy of U.S. Patent No. 5,227,996's front page, which bears this information, is attached hereto as Exhibit M. Also attached as Exhibit N is a declaration signed by Toshiya Uchida confirming under penalty of perjury the inventor's residence in Japan.

10. U.S. Patent No. 5,339,273 identifies Masao Taguchi as the sole inventor and Fujitsu Limited as the assignee. Masao Taguchi is identified as residing in Kawasaki, Japan, and Fujitsu Limited is identified as residing in Kanagawa, Japan. A true and correct copy of U.S. Patent No. 5,339,273's front page, which bears this information, is attached hereto as Exhibit O. Also attached as Exhibit P is a declaration signed by Masao Taguchi confirming under penalty of perjury the inventor's residence in Japan.

11. U.S. Patent No. 5,397,432 identifies Jun-ichi Konno, Keisuke Shinagawa, Toshiyuki Ishida, Takahiro Ito, Tetsuo Kondo, Fukashi Harada, and Shuzo Fujimura as the inventors and Fujitsu Limited as the assignee. Jun-ichi Konno is identified as residing in Kuwana, Japan, Keisuke Shinagawa is identified as residing in Kawasaki, Japan, Toshiyuki Ishida is identified as residing in Kawasaki, Japan, Takahiro Ito is identified as residing in Kawasaki, Japan, Tetsuo Kondo is identified as residing in Kawasaki, Japan, Fukashi Harada is identified as residing in Kuwana, Japan, Shuzo Fujimura is identified as residing in Tokyo, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 5,397,432's front page, which bears this information, is attached hereto as Exhibit Q. Also attached as Exhibit R is a declaration signed by Jun-ichi Konno confirming under penalty of perjury the inventor's residence in Japan.

12. U.S. Patent No. 5,688,712 identifies Taiji Ema and Toshimi Ikeda as the inventors and Fujitsu Limited as the assignee. Taiji Ema is identified as residing in Kawasaki, Japan, Toshimi Ikeda is identified as residing in Kawasaki, Japan, and Fujitsu Limited is identified as residing in Kanagawa, Japan. A true and correct copy of U.S. Patent No. 5,688,712's front page, which bears this information, is attached hereto as Exhibit S. Also attached as Exhibit T is a declaration signed by Taiji Ema confirming under penalty of perjury the inventor's residence in Japan.

13. U.S. Patent No. 5,841,731 identifies Naoharu Shinozaki as the sole inventor and Fujitsu Limited as the assignee. Naoharu Shinozaki is identified as residing in Kawasaki, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 5,841,731's front page, which bears this information, is attached hereto as Exhibit U. Also attached as Exhibit V is a declaration signed by Naoharu Shinozaki confirming under penalty of perjury the inventor's residence in Japan.

14. U.S. Patent No. 6,104,486 identifies Hiroshi Arimoto as the sole inventor and Fujitsu Limited as the assignee. Hiroshi Arimoto is identified as residing in Kawasaki, Japan, and Fujitsu

Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 6,104,486's front page, which bears this information, is attached hereto as Exhibit W.

15. U.S. Patent No. 6,292,428 identifies Hiroyoshi Tomita and Tatsuya Kanda as the inventors and Fujitsu Limited as the assignee. Hiroyoshi Tomita is identified as residing in Kawasaki, Japan, Tatsuya Kanda is identified as residing in Kawasaki, Japan, and Fujitsu Limited is identified as residing in Kanagawa, Japan. A true and correct copy of U.S. Patent No. 6,292,428's front page, which bears this information, is attached hereto as Exhibit X. Also attached as Exhibit Y is a declaration signed by Hiroyoshi Tomita and Tatsuya Kanda confirming under penalty of perjury each inventor's residence in Japan.

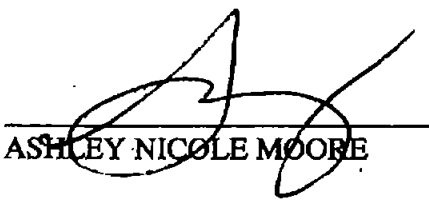
16. U.S. Patent No. 6,320,819 identifies Hiroyoshi Tomita and Tatsuya Kanda as the inventors and Fujitsu Limited as the assignee. Hiroyoshi Tomita is identified as residing in Kawasaki, Japan, Tatsuya Kanda is identified as residing in Kawasaki, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 6,320,819's front page, which bears this information, is attached hereto as Exhibit Z. Also attached as Exhibit AA is a declaration signed by Hiroyoshi Tomita and Tatsuya Kanda confirming under penalty of perjury each inventor's residence in Japan.

17. I personally obtained and confirmed all of the foregoing information from records retrieved from the United States Patent and Trademark Office.

18. Upon and information and belief, Defendant Fujitsu Limited, is a Japanese corporation, having its principal place of business at Shiodome City Center, 1-5-2 Higashi-Shimbashi, Minato-ku, Tokyo 105-7123, Japan.

19. Upon and information and belief, Defendant Fujitsu Microelectronics America, Inc. is a wholly owned subsidiary of Fujitsu Ltd. and is headquartered and has its principal place of business at 1250 E. Arques Avenue, M/S 333, Sunnyvale, California 94088-3470.

I DECLARE UNDER PENALTY OF PERJURY THAT THE FOREGOING IS TRUE AND CORRECT. SIGNED THIS FIRST DAY OF MAY, 2007.



ASHLEY NICOLE MOORE

United States Patent [19]

Abe

[11] **4,384,918**

[45] **May 24, 1983**

[54] **METHOD AND APPARATUS FOR DRY ETCHING AND ELECTROSTATIC CHUCKING DEVICE USED THEREIN**

[75] Inventor: **Naomichi Abe, Tokyo, Japan**

[73] Assignee: **Fujitsu Limited, Kawasaki, Japan**

[21] Appl. No.: **304,902**

[22] Filed: **Sep. 23, 1981**

[30] **Foreign Application Priority Data**

Sep. 30, 1980 [JP] Japan 55-136255
Oct. 8, 1980 [JP] Japan 55-141046

[51] Int. Cl.³ C23C 15/00

[52] U.S. Cl. ..... 156/643; 156/345; 204/192 E; 204/298; 361/234

[58] Field of Search ..... 156/345, 643; 204/192 E, 298; 279/1 R, 1 M; 271/18.1, 18.2, 193; 198/691; 361/234; 118/500

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,634,740	1/1972	Stenzko	361/234
3,916,270	10/1975	Wachtuer et al.	361/234
4,184,188	1/1980	Briglia	361/234
4,282,267	8/1981	Kuyel	204/192 E
4,292,153	9/1981	Kudo et al.	204/298
4,313,783	2/1980	Davies et al.	156/345
4,324,611	4/1982	Vogel et al.	204/298

OTHER PUBLICATIONS

"Microetch Ion Beam Milling", VEECO Co. Catalog, pp. 1–29.

"Wafer Coaling . . . Etching", Conference Paper of Precision Machine Society, (1979), pp. 193–194.

Primary Examiner—Jerome W. Massie
Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

An electrostatic chucking device is positioned on a supporting base, the temperature of which is maintained at a predetermined value, the device having an insulator, and a pair of plane electrodes on the insulator, and a material being chucked on the bottom surface of the top surface of the insulator, wherein the sum of the area of portions of the pair of plane electrodes facing the direction of the material being approximately equal to the contact area between the material and the insulator, and wherein a voltage is applied between the plane electrodes from an external power source, thereby effectively electrostatically chucking the material to the supporting base. A method and an apparatus for dry etching of a material having at least a conductive portion therein, the material being chucked by using said electrostatic chucking device mounted on a supporting base, the temperature of which is maintained at a predetermined value, in at least one of a sputter etching apparatus, a reactive sputter etching apparatus, or a plasma etching apparatus, whereby the material is indirectly chucked to the supporting base, the heat conductivity between the material and the supporting base is increased, the temperature of the material is controlled effectively, and the material can be held invertedly in the horizontal plane or vertically.

18 Claims, 10 Drawing Figures

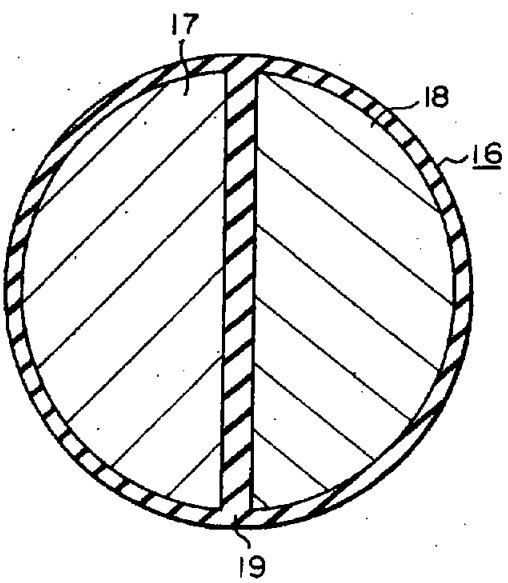


EXHIBIT A

United States Patent [19]

Takemae

[11] **Patent Number: 4,458,336**

[45] **Date of Patent: Jul. 3, 1984**

[54] **SEMICONDUCTOR MEMORY CIRCUIT**

[75] Inventor: Yoshihiro Takemae, Yokohama, Japan

[73] Assignee: Fujitsu Limited, Kawasaki, Japan

[21] Appl. No.: 313,616

[22] Filed: Oct. 21, 1981

[30] Foreign Application Priority Data

Oct. 22, 1980 [JP] Japan 55-147771
Oct. 22, 1980 [JP] Japan 55-147773

[51] Int. Cl.³ G11C 11/40
[52] U.S. Cl. 365/149; 365/203
[58] Field of Search 365/149, 154, 190, 202, 365/203, 205, 207, 222

[56] References Cited

U.S. PATENT DOCUMENTS

4,045,783 8/1977 Harland 365/149
4,195,357 3/1980 Kuo et al. ..... 365/149 X
4,291,393 9/1981 Wilson 365/203

Primary Examiner—Joseph A. Popek
Attorney, Agent, or Firm—Staas & Halsey

[57] ABSTRACT

A semiconductor memory circuit is disclosed, which includes: word lines, bit lines and memory cells at each cross point of the word lines and the bit lines. Each memory cell including a capacitor, having a first electrode and a second electrode, and a transfer-gate transistor connected in series with the capacitor at the first electrode thereof. The memory circuit also includes pre-charge circuits each charging one corresponding bit line to a predetermined pre-charge voltage level by using a memory power source and sense amplifiers each amplifying the voltage level developed at one corresponding bit line so as to have a high voltage level or a low voltage level in accordance with the charge stored in each corresponding capacitor. Additionally included are a first circuit which supplies the pre-charge voltage to the pre-charge circuit, the level of the pre-charge voltage is in the middle between the high voltage level and the low voltage level, and a second circuit which supplies a predetermined voltage to the capacitor at its second electrode. Preferably the predetermined voltage supplied from the second circuit is same as the voltage supplied from the first circuit.

12 Claims, 15 Drawing Figures

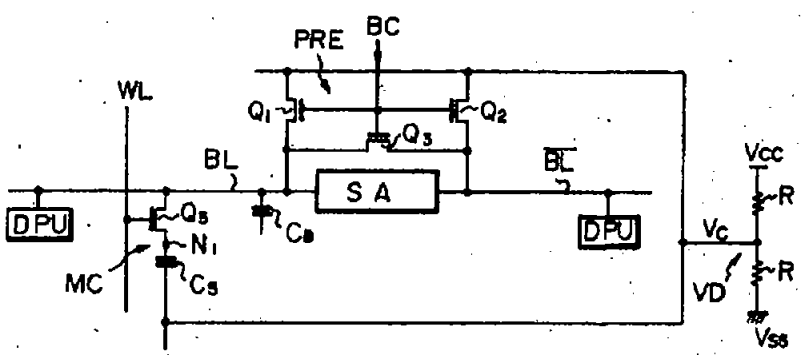


EXHIBIT B

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを特許商標庁に対して遂行する弁護士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

And I hereby appoint as principal attorneys: David T. Nikaido, Reg. No. 22,663; Charles M. Marmelstein, Reg. No. 25,895; George B. Oram, Jr., Reg. No. 27,931; Robert B. Murray, Reg. No. 22,980; E. Marcie Emas, Reg. No. 32,131; Douglas H. Goldhush, Reg. No. 33,125; Monica Chin Kim, Reg. No. 36,105; Richard J. Berman, Reg. No. 39,107; King L. Wong, Reg. No. 37,500; Karen K. Cosentino, Reg. No. 35,107; James A. Peslos, III, Reg. No. 31,714; Patrick D. Muir, Reg. No. 37,405; Sharon N. Kleiner, Reg. No. 36,335; and Marat Otgaz, Reg. No. 44,275; Bradley D. Goldkrand, Reg. No. 43,637; and N. Alexander Neiss, Reg. No. 45,489.

書類送付先

Please direct all communications to the following address:
ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W., Suite 600
Washington, D.C. 20036-5339
Tel: (202) 857-6000; Fax: (202) 857-6395

唯一または第一発明者名		Full name of sole or first inventor	Yoshihiro Takemae
発明者の署名	日付	Inventor's signature	Date Jan. 21, 2002
住所		Residence	Kasugai, Japan
国籍		Citizenship	JAPAN
私書箱		Post Office Address	c/o FUJITSU VLSI LIMITED 1844-2, Kozoji-cho 2-chome, Kasugai-shi, Aichi 487-0013 Japan
第二共同発明者名		Full name of second joint inventor, if any	
第二共同発明者の署名	日付	Second inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	

（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)

EXHIBIT C

United States Patent [19]

Matsui et al.

[11] **Patent Number: 4,527,070**

[45] **Date of Patent: Jul. 2, 1985**

[54] **METHOD AND APPARATUS FOR INSPECTING A PATTERN**

[75] Inventors: Shougo Matsui, Sagamihara; Yoshimitu Mashima, Kawasaki; Kenichi Kobayashi, Tokyo, all of Japan

[73] Assignee: Fujitsu Limited, Kawasaki, Japan

[21] Appl. No.: 409,983

[22] Filed: Aug. 20, 1982

[30] **Foreign Application Priority Data**

Aug. 20, 1981 [JP] Japan 56-131276

[51] Int. Cl.³ G01N 21/86

[52] U.S. Cl. 250/560; 356/376

[58] Field of Search 364/468, 488–491; 250/556, 560; 358/101, 106; 356/400, 376

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,318,081	3/1982	Yoshida	364/468
4,390,955	6/1983	Arimura	358/101
4,414,566	11/1983	Peyton et al.	358/101
4,445,137	4/1984	Panofsky	358/101

Primary Examiner—David C. Nelms
Assistant Examiner—J. Jon Brophy
Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

In a method for inspecting a pattern produced by using pattern data of a predetermined reference pattern, comparison is carried out between the pattern reproduced from the scanning signal of the pattern and the pattern produced from the signal of a modified form of the predetermined reference pattern.

12 Claims, 8 Drawing Figures

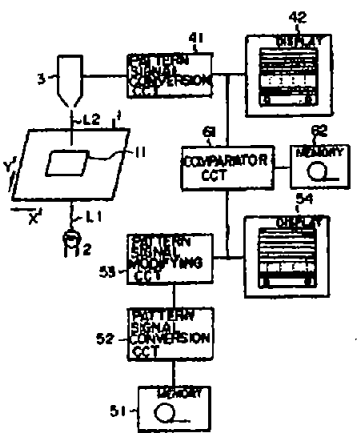


EXHIBIT D

FJ-3535-US

Dkt. No. 22.1550/CMK

SUPPLEMENTAL DECLARATION AFTER ALLOWANCE

We, SHOUGO MATSUI, YOSHIMITU MASHIMA and KENICHI KOBAYASHI, residing at 1609-33, Sobudaidanchi, Sagamihara-shi, Kanagawa 229, Japan; Suehiroso, 1743, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211, Japan and 6-34-3, Nagasaki, Toshima-ku, Tokyo 171, Japan, declare that we are citizens of JAPAN and we are the same individuals who on or about August 11, 1982 executed a combined Declaration and Power of Attorney accompanying the subject U.S. Patent Application entitled METHOD AND APPARATUS FOR INSPECTING A PATTERN, which was filed August 20, 1982 and assigned U.S. Serial No. 409,983. We have reviewed and understand the amendments to the subject application, and we declare that we are the original and first inventors of the invention as now described and claimed therein.

We declare that all statements made herein of our own knowledge are true, that all statements made on information and belief are believed to be true, that these statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the subject application or any patent issuing thereon.

Dated April 4, 1985

Shougo Matsui
SHOUGO MATSUI

Dated April 4, 1985

Yoshimitu Mashima
YOSHIMITU MASHIMA

Dated April 4, 1985

Kenichi Kobayashi
KENICHI KOBAYASHI

EXHIBIT
E

United States Patent [19]

Takagi et al.

[11] **Patent Number: 4,539,068**

[45] **Date of Patent: Sep. 3, 1985**

[54] **VAPOR PHASE GROWTH METHOD**

[75] Inventors: **Miklo Takagi, Kawasaki; Kanetake Takasaki, Tokyo; Kenji Koyama, Yokosuka, all of Japan**

[73] Assignee: **Fujitsu Limited, Kawasaki, Japan**

[21] Appl. No.: **412,260**

[22] Filed: **Aug. 27, 1982**

Related U.S. Application Data

[63] Continuation of Ser. No. 264,805, May 18, 1981, abandoned, which is a continuation-in-part of Ser. No. 184,363, Sep. 5, 1980, abandoned.

[30] **Foreign Application Priority Data**

Sep. 20, 1979 [JP] Japan 54-121489

[51] Int. Cl.³ C30B 25/02

[52] U.S. Cl. 156/614; 427/93; 427/94; 156/DIG. 64

[58] Field of Search ..... 156/614, 613, DIG. 64, 156/DIG. 99; 423/349; 148/175; 427/34, 39, 86, 94, 93, 95, 248.1, 255.2, 87; 204/192 S, 177, 164

[56] **References Cited**

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3,600,126	8/1971	Hallund	422/23
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4,173,661	11/1979	Bourdon	427/39

Primary Examiner—Hiram H. Bernstein
Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

A plasma chemical vapor deposition method for forming a film on a substrate which is placed on one of a pair of electrodes oppositely arranged within the reaction chamber of a reactor. A plurality of power generators of different frequencies are applied to the electrodes to excite reactive gases introduced into the reaction chamber, whereby the reactive gases are transformed into a plasma and a desired film is formed on the substrate. Film with a small number of pinholes was formed at a relatively high deposition rate by combinations of power generator frequencies of, for example, 13.56 MHz and 1 MHz, 13.56 MHz and 50 KHz, and 5 MHz and 400 KHz.

3 Claims, 10 Drawing Figures

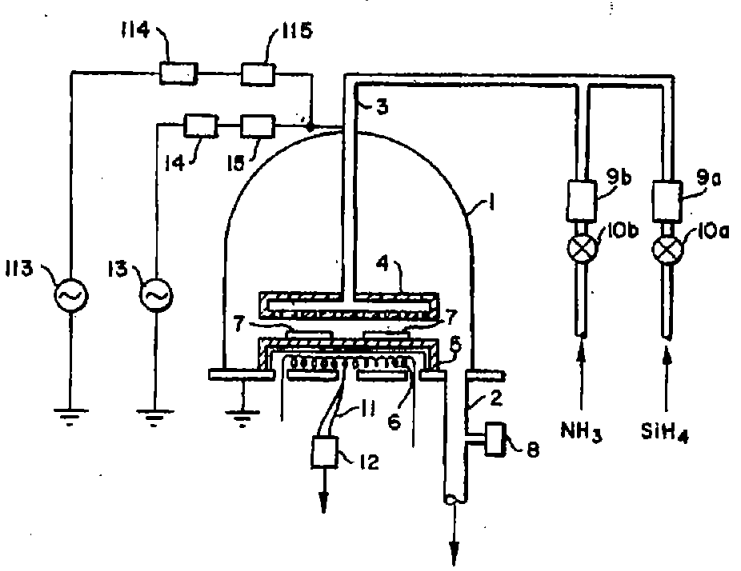

EXHIBIT F

Dkt. No. 21.1071-CIP/C/JCG

SUPPLEMENTAL DECLARATION AFTER ALLOWANCE

We, MIKIO TAKAGI, KANETAKE TAKASAKI and KENJI KOYAMA, residing at 6-20-3, Nagao, Tama-ku, Kawasaki-shi, Kanagawa 213, Japan; 2-26-10-703, Ohmorikita, Ohta-ku, Tokyo 143, Japan; and 3-56, Higashihemi-cho, Yokosuka-shi, Kanagawa 238, Japan, declare that we are citizens of JAPAN and we are the same individuals who on or about May 13, 1981 executed a combined Declaration and Power of Attorney accompanying the subject U.S. Patent Application S.N. 264,805 entitled VAPOR PHASE GROWTH METHOD AND APPARATUS, which was filed on May 18, 1981 which is a continuation-in-part of U.S. Serial No. 184,363 filed September 5, 1980, the subject application being a continuation of U.S. Serial No. 264,805, assigned U.S. Serial No. 412,260 and filed August 27, 1982. We have reviewed and understand the amendments to the above applications, and we declare that we are the original and first inventors of the invention as now described and claimed therein.

We declare that all statements made herein of our own knowledge are true, that all statements made on information and belief are believed to be true, that these statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the subject application or any patent issuing thereon.

Dated June 5, 1985 — Mikio Takagi
MIKIO TAKAGI

Dated June 5, 1985 — Kanetake Takasaki
KANETAKE TAKASAKI

Dated June 5, 1985 — Kenji Koyama
KENJI KOYAMA

EXHIBIT G

United States Patent [19]

Takemae et al.

[11] **Patent Number: 4,641,166**

[45] **Date of Patent: Feb. 3, 1987**

[54] **SEMICONDUCTOR MEMORY DEVICE HAVING STACKED CAPACITOR-TYPE MEMORY CELLS**

[75] Inventors: **Yoshihiro Takemae, Tokyo; Tomio Nakano, Kawasaki; Kimiaki Sato, Tokyo, all of Japan**

[73] Assignee: **Fujitsu Limited, Kawasaki, Japan**

[21] Appl. No.: **560,171**

[22] Filed: **Dec. 12, 1983**

[30] **Foreign Application Priority Data**

Dec. 20, 1982 [JP] Japan 57-222079

[51] Int. Cl.⁴ H01L 29/78

[52] U.S. Cl. 357/23.6; 357/51; 357/54

[58] Field of Search 357/23.6, 23.11, 51, 357/24, 54

[56] **References Cited**

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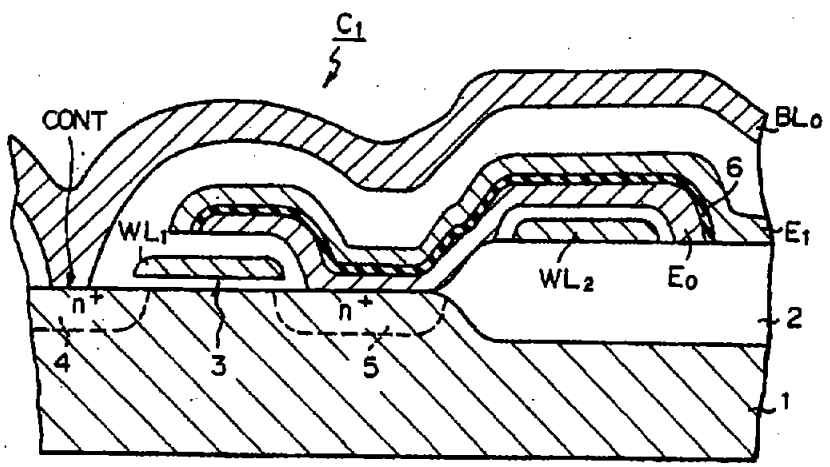
0021170	2/1980	Japan	357/23 C
55-154762	12/1980	Japan .	

Primary Examiner—Martin H. Edlow
Assistant Examiner—Sara W. Crane
Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

In a semiconductor memory device having stacked capacitor-type memory cells, the capacitor of each memory cell comprises an electrode, an insulating layer, and a counter electrode. The electrode is connected electrically to a source or drain region of a transfer transistor and extends over a part of a word line adjacent to another word line serving a gate electrode of the transfer transistor, at which part no memory cell is formed.

10 Claims, 8 Drawing Figures



FP-4819
FJ-4207-US

Docket No. 22.1786/WDJ

SUPPLEMENTAL DECLARATION AFTER ALLOWANCE

We, Yoshihiro Takemae, Tomio Nakano, Kimiaki Sato, residing at 8-13-24-303, Akasaka, Minato-ku, Tokyo 107, Japan; 3-1-27-103, Sugegengoku, Tama-ku, Kawasaki-shi, Kanagawa 214, Japan and 4-11-35-204, Minamiazabu, Minato-ku, Tokyo 106, Japan respectively, declare that we are citizens of Japan and that we are the same individuals who, on or about 25 November 1983 executed a combined Declaration and Power of Attorney accompanying a U.S. patent application entitled SEMICONDUCTOR MEMORY DEVICE HAVING STACKED CAPACITOR-TYPE MEMORY CELLS, which was filed 12 December 1983 and assigned Serial No. 560,171. We have read all amendments to the specification and claims of the application, we understand the content of the invention as now described and claimed in the subject application and we declare that we are the original and first inventors thereof and further that this invention was completed before the filing of the subject application.

We acknowledge our duty to disclose information of which we are aware which is material to the examination of the subject application.

EXHIBIT I

We declare further that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

September 1, 1986
Date

Yoshihiro Takemae
Yoshihiro Takemae

September 1, 1986
Date

Tomoio Nakano
Tomoio Nakano

September 1, 1986
Date

Kimiaki Sato
Kimiaki Sato

United States Patent [19]

Takemae

[11] Patent Number: 4,692,689

[45] Date of Patent: Sep. 8, 1987

[54] **FET VOLTAGE REFERENCE CIRCUIT WITH THRESHOLD VOLTAGE COMPENSATION**

[75] Inventor: Yoshihiro Takemae, Tokyo, Japan

[73] Assignee: Fujitsu Limited, Kawasaki, Japan

[21] Appl. No.: 15,529

[22] Filed: Feb. 12, 1987

Related U.S. Application Data

[63] Continuation of Ser. No. 663,712, Oct. 22, 1984, abandoned.

[30] **Foreign Application Priority Data**

Nov. 11, 1983 [JP] Japan 58-212083

[51] Int. Cl.[4] G05F 3/24

[52] U.S. Cl. 323/313; 307/297; 307/304; 323/314; 323/349; 323/350; 365/226

[58] Field of Search ..... 323/311, 313, 349, 350, 323/314; 307/296 R, 297, 304; 365/226

[56] **References Cited**

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29231	5/1981	European Pat. Off.	323/313
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Askin et al., "FET Device Parameters Compensation Circuit", IBM Tech. Discl. Bul., vol. 14, No. 7, pp. 2088, 2089, Dec. 1971.

Primary Examiner—William H. Beha, Jr.

Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

A voltage converting circuit has an output MIS transistor which gives a low output impedance and outputs an intermediate level of power source voltage. The output level is set with a high accuracy through a voltage dividing ratio determined by an impedance element. This impedance element is connected with a compensating MIS transistor to compensate for variations of the gate threshold voltage caused by the manufacturing process.

10 Claims, 9 Drawing Figures

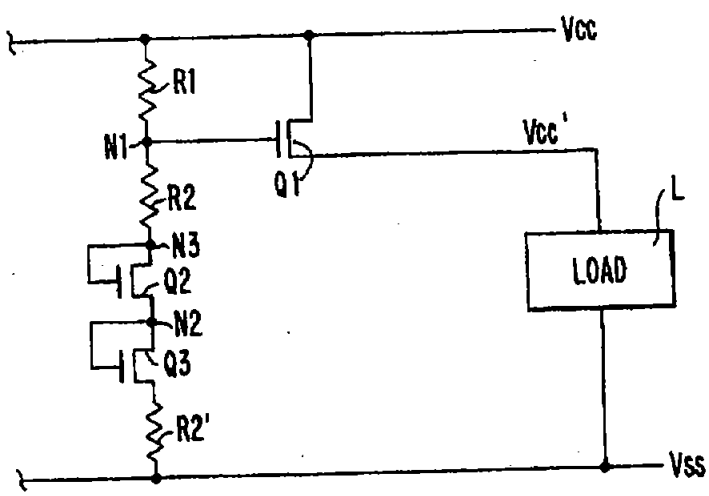

EXHIBIT J

United States Patent [19]

Taguchi

[11] **Patent Number: 4,801,989**

[45] **Date of Patent: Jan. 31, 1989**

[54] **DYNAMIC RANDOM ACCESS MEMORY HAVING TRENCH CAPACITOR WITH POLYSILICON LINED LOWER ELECTRODE**

[75] Inventor: **Masao Taguchi, Sagamihara, Japan**

[73] Assignee: **Fujitsu Limited, Kanagawa, Japan**

[21] Appl. No.: **16,611**

[22] Filed: **Feb. 19, 1987**

[30] **Foreign Application Priority Data**

Feb. 20, 1986 [JP] Japan 61-036361
Mar. 3, 1986 [JP] Japan 61-045822

[51] **Int. Cl.**[4] **H01C 29/78**

[52] **U.S. Cl.** **357/23.6**; 357/54; 357/55; 357/59; 365/149

[58] **Field of Search** 357/23.6, 55, 59, 54; 365/149

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,672,410 6/1987 Miura et al. 357/23.6

FOREIGN PATENT DOCUMENTS

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0171131 2/1986 European Pat. Off. .
59-213460 12/1983 Japan 357/23.6
59-141262 8/1984 Japan .
60-54472 of 1985 Japan .
61-15362 1/1986 Japan .

Primary Examiner—Joseph E. Clawson, Jr.
Attorney, Agent, or Firm—Armstrong, Nikaido, Marmelstein & Kubovcik

[57] **ABSTRACT**

In a dynamic random access memory having a trench capacitor, a first conductive layer is formed on all of the inner surface of the trench except for a region adjacent to the opening portion of the trench, a dielectric layer is formed on the first conductive layer exposed in the trench and the surface of the semiconductor substrate, and a second conductive layer of the other conduction type is filled in the trench through the dielectric layer. The first conductive layer, the dielectric layer, and the second conductive layer constitute a storage capacitor. In this dynamic random access memory, a metal insulator semiconductor transistor is formed in the semiconductor substrate, a source or drain region of the transistor of the other conduction type is in contact with the second conductive layer through the dielectric layer, and the second conductive layer is connected with the source or drain region of the other conduction type.

8 Claims, 9 Drawing Sheets

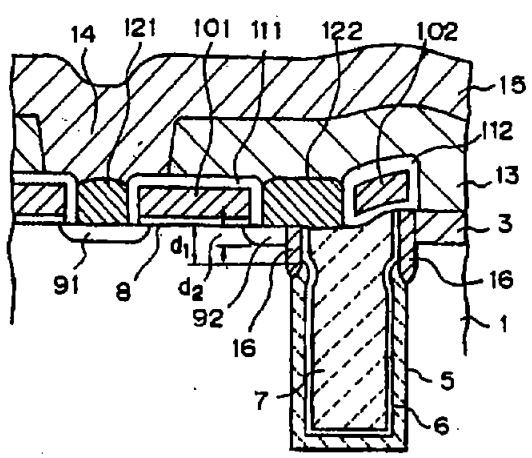

EXHIBIT K

ARMSTRONG, NIKAIDO, MARMELSTEIN & KUBOVCIK

FP-3965

Declaration For Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled DYNAMIC RANDOM ACCESS MEMORY HAVING TRENCH CAPACITOR, the specification of which

(check one) ☒ is attached hereto.

☐ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
61-036361(Pat. Appln.) (Number)	Japan (Country)	20/February/1986 (Day/Month/Year Filed)	☒ Yes ☐ No
61-045822(Pat. Appln.) (Number)	Japan (Country)	3/March/1986 (Day/Month/Year Filed)	☒ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

And I hereby appoint as principal attorneys James E. Armstrong, III, Reg. No. 18,266; David T. Nikaido, Reg. No. 22,663; Charles M. Marmelstein, Reg. No. 25,895; Ronald J. Kubovcik, Reg. No. 25,401; George E. Oram, Jr., Reg. No. 27,931; R. Eu... Jr., Reg. No. 29,728; C. Daniel Cornish, Reg. No. 19,240; Hubert E. Evans, Reg. No. 16,040.

Please direct all communications to the following address:

Armstrong, Nikaido, Marmelstein & Kubovcik
1725 K Street, N.W., Suite 912
Washington, D.C. 20006
(202) 659-2930

EXHIBIT
tabbies
L

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor Masao Taguchi

Inventor's signature Masao Taguchi

February 12, 1987
Date

Residence Sagamihara-shi, Kanagawa, Japan

Citizenship Japanese

Post Office Address 4-3-4-201, Araisono, Sagamihara-shi, Kanagawa 228, Japan

US005227996A

United States Patent [19]

Uchida

[11] Patent Number: 5,227,996

[45] Date of Patent: Jul. 13, 1993

[54] **SEMICONDUCTOR MEMORY DEVICE HAVING WORD LINE DRIVER**

[75] Inventor: Toshiya Uchida, Kawasaki, Japan

[73] Assignee: Fujitsu Limited, Kanagawa, Japan

[21] Appl. No.: 757,154

[22] Filed: Sep. 10, 1991

[30] Foreign Application Priority Data

Sep. 14, 1990 [JP] Japan 2-244585

[51] Int. Cl.[5] G11C 5/06

[52] U.S. Cl. 365/72; 365/63; 365/230.06

[58] Field of Search 365/63, 72, 230.06, 365/189.11

[56] References Cited

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4,694,428	9/1987	Matsumura et al.	365/63 X
4,782,465	11/1988	Uchida	365/72
4,992,981	2/1991	Gensslosar et al.	365/63 X

Primary Examiner—Eugene R. LaRoche

Assistant Examiner—Do Hyum Yoo

Attorney, Agent, or Firm—Nikaido, Marmelstein, Murray & Oram

[57] ABSTRACT

A semiconductor memory device includes first and second word lines which extend in parallel to each other, at least one line activation signal line which extends perpendicularly to the first and second word lines, a device isolation region which extends perpendicularly to the first and second word lines, a first driver for activating the first word line and having a first impurity region provided adjacent to the device isolation region and connected to the word line activation signal line, a first gate electrode and a second impurity region connected to the first word line, a second driver for activating the second word line and comprising a third impurity region provided adjacent to the device isolation region on an opposite side from the first impurity region and connected to the word line activation signal line, a second gate electrode and a fourth impurity region connected to the second word line, and a decoder connected to the first and second gate electrodes.

14 Claims, 8 Drawing Sheets

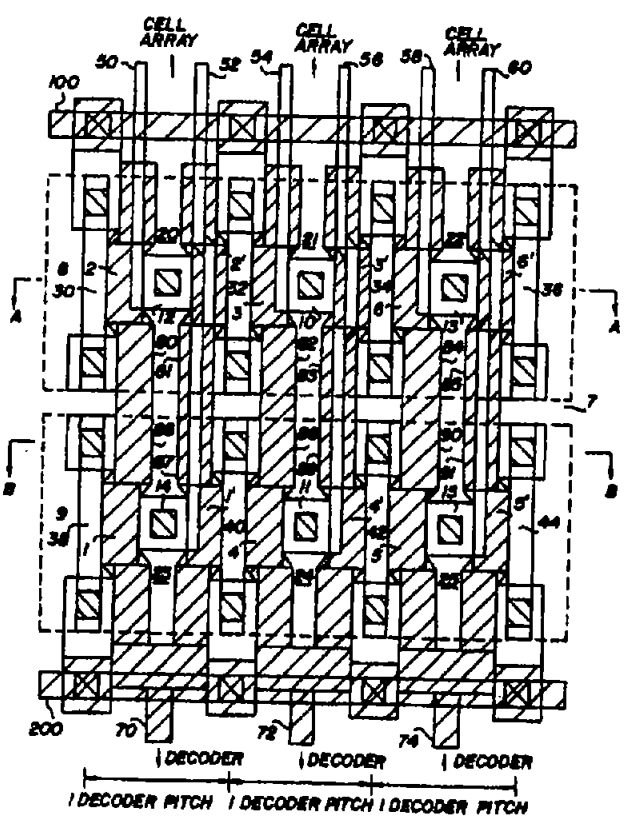

EXHIBIT M

Declaration for U.S. Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR MEMORY DEVICE HAVING WORD LINE DRIVER

the specification of which

(Check one of blocks 1, 2, or 3. See note A on back of this page)

1. ☒ is attached hereto.
2. ☐ was filed on _____ as International PCT Application Serial No. _____ and was amended on _____ (if applicable)
3. ☐ was filed on _____ as U.S. Application Serial No. _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application for which priority is claimed:

	(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
(List prior foreign applications. See note B on back of this page)	2-244585(Pat.Appln.)	Japan	14/September/1990	☒ Yes ☐ No
				☐ Yes ☐ No
				☐ Yes ☐ No
				☐ Yes ☐ No

(See Note C on back of this page) ☐ See attached list for additional prior foreign applications

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

	(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)
(List Prior U.S. Applications)			

And I hereby appoint as principal attorneys James E. Armstrong, III, Reg. No. 18,366; David T. Nikaido, Reg. No. 22,663; Charles M. Marmelstein, Reg. No. 25,895; Ronald J. Kubovcik, Reg. No. 25,401; George E. Oram, Jr., Reg. No. 27,931; Robert B. Murray, Reg. No. 22,980; William F. Westerman, Reg. No. 29,988; Kenichi Hattori, Reg. No. 32,861; John R. Pegan, Reg. No. 18,669; Martin S. Postman, Reg. No. 18,570; Le-Nhung McLeland, Reg. No. 31,541; J. Herbert O'Toole, Reg. No. 31,404; James P. Welch, Reg. No. 17,379; E. Marcie Emas, Reg. No. 32,131; Ronald F. Naughton, Reg. No. 24,616; Albert Tockman, Reg. No. 17,722; Mel R. Quinton, Reg. No. 31,898; Michael C. Gilman, Reg. No. 19,114; Michael J. Foycik, Jr., Reg. No. 30,928; Cynthia Lee Foulke, Reg. No. 31,364; James C. Lydon, Reg. No. 30,082; Douglas H. Goldhush, Reg. No. 33,125.

Please direct all communications to the following address:

ARMSTRONG, NIKAIDO, MARMELSTEIN, KUBOVCIK & MURRAY
1725 K Street, N.W., Suite 1000
Washington, D.C. 20006
(202) 659-2930 Fax: (202) 887-0357

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

(See Note D on back of this page)

Full name of sole or first inventor: Toshiya Uchida

Inventor's signature: Toshiya Uchida Date: September 2, 1991

Residence: c/o FUJITSU LIMITED 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211 Japan

Citizenship: Japan

Post Office Address: same as residence

EXHIBIT N

US005339273A

United States Patent [19]

Taguchi

[11] Patent Number: 5,339,273

[45] Date of Patent: Aug. 16, 1994

[54] **SEMICONDUCTOR MEMORY DEVICE HAVING A TESTING FUNCTION AND METHOD OF TESTING THE SAME**

[75] Inventor: **Masao Taguchi**, Kawasaki, Japan

[73] Assignee: **Fujitsu Ltd.**, Kanagawa, Japan

[21] Appl. No.: **806,406**

[22] Filed: **Dec. 13, 1991**

[30] **Foreign Application Priority Data**

Dec. 14, 1990 [JP] Japan 2-410668

[51] Int. Cl.[5] G11C 29/00; G11C 7/00

[52] U.S. Cl. 365/201; 365/149; 365/205

[58] Field of Search 365/149, 200, 201, 184, 365/205; 371/21.1

[56] **References Cited**

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58-128077 7/1983 Japan .
62-84499 4/1987 Japan .
62-86600 4/1987 Japan .
63-140498 6/1988 Japan .
2-143984 6/1990 Japan .

Primary Examiner—Eugene R. LaRoche
Assistant Examiner—Son Dinh
Attorney, Agent, or Firm—Armstrong, Westerman, Hattori, McLeland & Naughton

[57] **ABSTRACT**

A semiconductor memory device is provided with a plurality of bit lines, a plurality of word lines, a memory cell array including a plurality of memory cells each coupled to one bit line and one word line, and a varying part for varying a capacitance of at least a selected one of the bit lines in response to a predetermined signal which indicates a test mode in which an operation of the semiconductor memory device is tested.

15 Claims, 7 Drawing Sheets

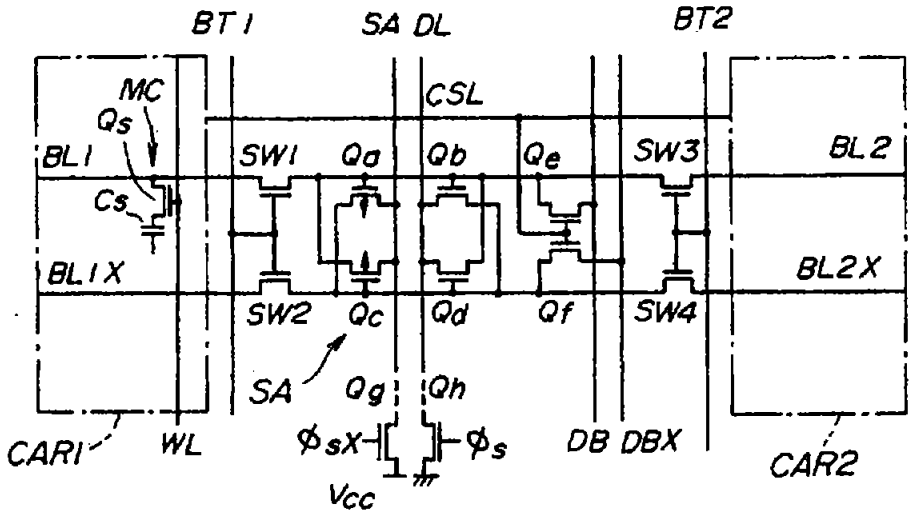

EXHIBIT O

Declaration For U.S. Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR MEMORY DEVICE HAVING A TESTING FUNCTION AND A METHOD OF TESTING THE SAME

the specification of which

(Check one of blocks 1, 2, or 3. See note A on back of this page)

1. ☒ is attached hereto.
2. ☐ was filed on _____ as International PCT Application Serial No. _____ and was amended on _____ (if applicable)
3. ☐ was filed on _____ as U.S. Application Serial No. _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application for which priority is claimed:

(List prior foreign applications. See note B on back of this page)	(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
	2-410668(Pat.Appln.)	Japan	14/December/1990	☒ Yes ☐ No
				☐ Yes ☐ No
				☐ Yes ☐ No
				☐ Yes ☐ No

(See Note C on back of this page) ☐ See attached list for additional prior foreign applications

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(List Prior U.S. Applications)	(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)

And I hereby appoint as principal attorneys James E. Armstrong, III, Reg. No. 18,386; David T. Nikaido, Reg. No. 22,663; Charles M. Marmelstein, Reg. No. 25,895; Ronald J. Kubovcik, Reg. No. 25,401; George R. Orara, Jr., Reg. No. 27,931; Robert E. Murray, Reg. No. 22,980; William F. Westerman, Reg. No. 29,988; Ken-Ichi Hattori, Reg. No. 32,861; John R. Fugea, Reg. No. 18,387; Martin S. Postman, Reg. No. 19,479; Le-Nhung McLeland, Reg. No. 31,541; J. Herbert O'Toole, Reg. No. 31,404; James P. Welch, Reg. No. 17,370; E. Marcie Emas, Reg. No. 32,131; Ronald F. Naughton, Reg. No. 31,616; Albert Rockman, Reg. No. 17,182; Mel R. Quinton, Reg. No. 31,868; Michael G. Gilman, Reg. No. 19,114; Michael J. Foycik, Jr., Reg. No. 30,928; Cynthia Lea Foulke, Reg. No. 32,364; James C. Lydon, Reg. No. 30,082; Douglas H. Goldhush, Reg. No. 33,125.

Please direct all communications to the following address:

ARMSTRONG, NIKAIDO, MARMELSTEIN,
KUBOVCIK & MURRAY
1725 K Street, N.W., Suite 1000
Washington, D.C. 20006
(202) 659-2930 Fax: (202) 887-0357

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

(See Note D on back of this page)

Full name of sole or first inventor: Masao Taguchi

Inventor's signature: Masao Taguchi Date: December 2, 1991

Residence: c/o FUJITSU LIMITED 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211 Japan JPX

Citizenship: Japan

Post Office Address: same as residence

EXHIBIT P

US005397432A

United States Patent [19]

Konno et al.

[11] Patent Number: 5,397,432

[45] Date of Patent: Mar. 14, 1995

[54] METHOD FOR PRODUCING SEMICONDUCTOR INTEGRATED CIRCUITS AND APPARATUS USED IN SUCH METHOD

[75] Inventors: Jun-ichi Konno, Kuwana; Keisuke Shinagawa, Kawasaki; Toshiyuki Ishida, Kawasaki; Takahiro Ito, Kawasaki; Tetsuo Kondo, Kawasaki; Fukashi Harada, Kuwana; Shuzo Fujimura, Tokyo, all of Japan

[73] Assignee: Fujitsu Limited, Kawasaki, Japan

[21] Appl. No.: 743,383

[22] PCT Filed: Jan. 26, 1991

[86] PCT No.: PCT/JP91/00861

§ 371 Date: Aug. 21, 1991

§ 102(e) Date: Aug. 21, 1991

[87] PCT Pub. No.: WO92/00601

PCT Pub. Date: Jan. 9, 1992

[30] Foreign Application Priority Data

Jun. 27, 1990 [JP] Japan 2-171791

[51] Int. Cl.[6] H01L 21/00

[52] U.S. Cl. 156/665; 156/643; 156/646; 134/1

[58] Field of Search 156/643, 646, 664, 665, 156/666; 134/1

[56] References Cited

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1-48421	2/1989	Japan .
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Japanese Patent Abstract of JP-A-1 251 742 (Jan. 1989).

Primary Examiner—R. Bruce Breneman

Assistant Examiner—George Goudreau

Attorney, Agent, or Firm—Nikaido, Marmelstein, Murray & Oram

[57] ABSTRACT

To prevent after-corrosion of wiring or electrodes formed by patterning films of aluminum or an alloy thereof by reactive ion etching (RIE) using an etchant containing chlorine gas or its gaseous compounds, residual chlorine on the surface of the wiring or electrodes is removed by exposing it to a plasma generated in an atmosphere containing water vapor or to neutral active species extracted from the plasma. This treatment is performed either at the same time or after an ashing operation, an operation for removing a resist mask used in the aforesaid RIE by adding water vapor to an atmosphere containing oxygen. To perform the latter separate treatment, an automatic processing system is disclosed in which an after-treatment apparatus for removing residual chlorine is connected, via a second load lock chamber, to an ashing apparatus connected to a RIE apparatus by a load lock chamber which is capable of making a vacuum.

19 Claims, 6 Drawing Sheets

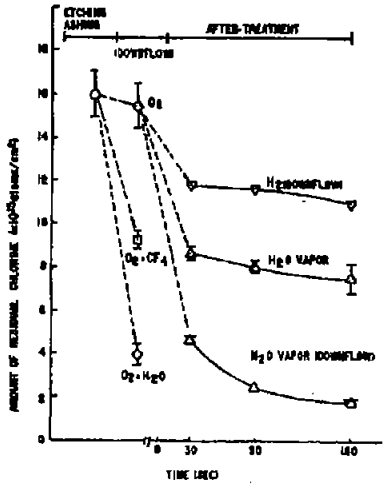

EXHIBIT Q

Declaration For U.S. Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD FOR PRODUCING SEMICONDUCTOR INTEGRATED CIRCUITS AND APPARATUS USED IN SUCH METHOD
the specification of which

(Check one of blocks 1, 2, or 3. See note A on back of this page)

1. ☐ is attached hereto.
2. ☒ was filed on June 26, 1991 as International PCT Application Serial No. PCT/JP91/00861 and was amended on _____ (if applicable)
3. ☐ was filed on _____ as U.S. Application Serial No. _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application for which priority is claimed:

(List prior foreign applications. See note B on back of this page)	(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
	2-171791	Japan	27/June/1990	☒ Yes ☐ No
				☐ Yes ☐ No
				☐ Yes ☐ No
				☐ Yes ☐ No

(See Note C on back of this page) ☐ See attached list for additional prior foreign applications

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(List Prior U.S. Applications)	(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)

And I hereby appoint as principal attorneys James E. Armstrong, III, Reg. No. 18,886; David T. Nikaido, Reg. No. 22,663; Charles M. Marmelstein, Reg. No. 25,895; Ronald J. Kubovcik, Reg. No. 25,401; George E. Oram, Jr., Reg. No. 27,931; Robert B. Murray, Reg. No. 22,980; William F. Westerman, Reg. No. 29,988; Martin S. Postman, Reg. No. 18,670; Le Nhung McLeland, Reg. No. 31,641; J. Herbert O'Toole, Reg. No. 31,404; James P. Welch, Reg. No. 17,379; E. Marcie Emas, Reg. No. 32,131; Scott M. Daniels, Reg. No. 32,562; Ronald F. Naughton, Reg. No. 24,616; Albert Tockman, Reg. No. 19,723; James A. Poulos, Reg. No. 31,714; Mel R. Quintos, Reg. No. 31,898; Hubert E. Evans, Reg. No. 15,040; Michael G. Gilman, Reg. No. 19,114.

Please direct all communications to the follwing address:

ARMSTRONG, NIKAIDO, MARMELSTEIN,
KUBOVCIK & MURRAY
1725 K Street, N.W., Suite 1000
Washington, D.C. 20006
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statments were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

(See Note D on back of this page)

Full name of sole or first inventor Jun-ichi Konno

Inventor's signature Junichi Konno Date July 26, 1991

Residence AZ house 205, 327-3, Higashikata, Kuwana-shi, Mie, 511 Japan

Citizenship Japan

Post Office Address Same as residence above

EXHIBIT R

US005688712A

United States Patent [19]

Ema et al.

[11] Patent Number: 5,688,712

[45] Date of Patent: Nov. 18, 1997

[54] **PROCESS FOR PRODUCING A SEMICONDUCTOR DEVICE**

[75] Inventors: **Taiji Ema**; **Toshimi Ikeda**, both of Kawasaki, Japan

[73] Assignee: **Fujitsu Limited**, Kanagawa, Japan

[21] Appl. No.: **643,938**

[22] Filed: **May 7, 1996**

Related U.S. Application Data

[62] Division of Ser. No. 376,082, Jan. 20, 1995, Pat. No. 5,550,395, which is a continuation of Ser. No. 46,149, Apr. 15, 1993, abandoned.

[30] **Foreign Application Priority Data**

Apr. 16, 1992 [JP] Japan 4-096726
Oct. 9, 1992 [JP] Japan 4-271622

[51] Int. Cl.[6] H01L 21/70

[52] U.S. Cl. 437/60; 437/52; 437/49; 437/195; 437/228; 437/236

[58] Field of Search 437/60, 47, 48, 437/49, 51, 52, 189, 195, 228, 235, 236

[56] **References Cited**

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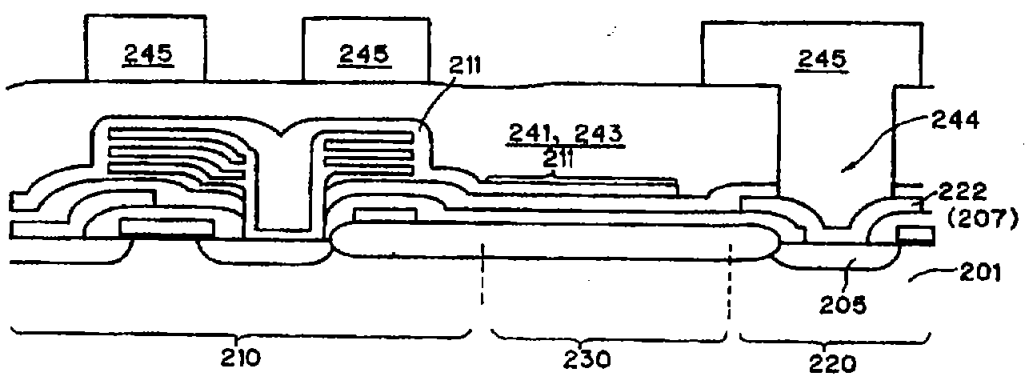
Primary Examiner—Tuan H. Nguyen
Attorney, Agent, or Firm—Nikaido Marmelstein Murray & Oram LLP

[57] **ABSTRACT**

A semiconductor device includes a semiconductor substrate having a memory cell area and a circuit area surrounding the memory cell area with a boundary area interposed therebetween. A first conductive layer covers the memory cell area and extends onto the boundary area. A first insulating layer covers the surrounding circuit area and part of the extended portion of the first conductive layer. A second insulating layer covering the first insulating layer and the first conductive layer. A throughhole is formed through the first and second insulating layers. A second conductive layer is electrically connected with another conductive layer via the throughhole and extends from the memory cell area to the surrounding circuit area. The process of producing the semiconductor device is also disclosed.

8 Claims, 18 Drawing Sheets



08/643938

N, M, M & O Docket No. _____ NIKAIDO, MARMELSTEIN, MURRAY & ORAM 9-P4036

Declaration For U.S. Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled (Insert Title) SEMICONDUCTOR DEVICE AND PROCESS OF PRODUCING SAME

the specification of which

(Check one of blocks 1, 2, or 3. See note A on back of this page)

1. ☒ is attached hereto.
2. ☐ was filed on _____ as International PCT Application Serial No. _____ and was amended on _____ (if applicable)
3. ☐ was filed on _____ as U.S. Application Serial No. _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application for which priority is claimed:

	(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
	04-096726(Pat. Appln.)	Japan	16/April/1992	☒ Yes ☐ No
	04-271622(Pat. Appln.)	Japan	9/October/1992	☒ Yes ☐ No
(List prior foreign applications. See note B on back of this page)				☐ Yes ☐ No
				☐ Yes ☐ No

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(List Prior U.S. Applications)	(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)
	(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)

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Please direct all communications to the following address:

NIKAIDO, MARMELSTEIN, MURRAY & ORAM
Metropolitan Square
655 Fifteenth Street, N.W., Suite 330 - G Street Lobby
Washington, D.C. 20005-5701
(202) 638-5000 Fax: (202) 638-4810

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1-00

(See Note D on back of this page)

Full name of sole or first inventor Taiji Ema

Inventor's signature Taiji Ema April 7, 1993 (Date)

Residence Kawasaki-shi, Kanagawa, Japan JPX

Citizenship Japanese

Post Office Address c/o FUJITSU LIMITED, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa 211 JPX

EXHIBIT T

US005841731A

United States Patent [19]

Shinozaki

[11] Patent Number: 5,841,731

[45] Date of Patent: Nov. 24, 1998

[54] **SEMICONDUCTOR DEVICE HAVING EXTERNALLY SETTABLE OPERATION MODE**

[75] Inventor: Naoharu Shinozaki, Kawasaki, Japan

[73] Assignee: Fujitsu Limited, Kawasaki, Japan

[21] Appl. No.: 862,298

[22] Filed: May 22, 1997

[30] Foreign Application Priority Data

Dec. 13, 1996 [JP] Japan 8-334273

[51] Int. Cl.[6] G11C 8/00

[52] U.S. Cl. 365/233; 365/191; 365/201; 365/230.08

[58] Field of Search 365/233, 191, 365/201, 230.08

[56] References Cited

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5,430,680	7/1995	Parris	365/222
5,525,331	6/1996	Kim	365/222

Primary Examiner—David C. Nelms
Assistant Examiner—Hien Nguyen
Attorney, Agent, or Firm—Nikaido, Marmelstein, Murray & Oram LLP

[57] ABSTRACT

A semiconductor device which allows an input signal thereto to select one of N operation modes, and operates in the one of N operation modes includes a selection circuit for selecting an operation mode from the N operation modes when the input signal indicates the operation mode, and for selecting a predetermined operation mode from the N operation modes when the input signal is an undefined signal indicating none of the N operation modes. The semiconductor device further includes an internal circuit operating in an operation mode selected by the selection circuit.

11 Claims, 8 Drawing Sheets

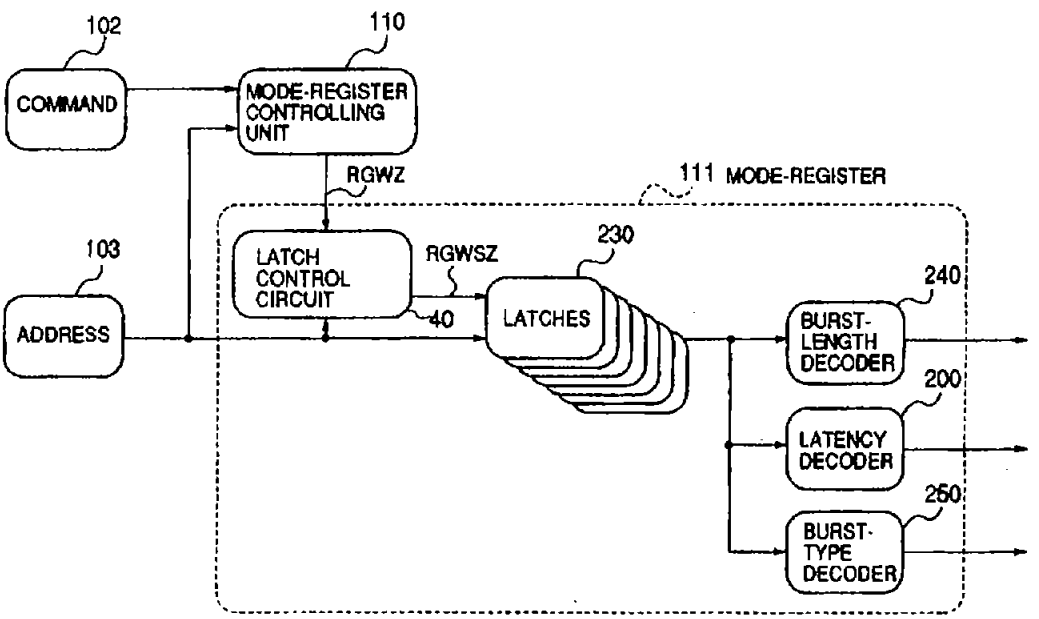

EXHIBIT U

N, M, M & O Docket No _____ NIK , MARMELSTEIN, MURRAY & ORA

Dec ation For U.S. Patent pplication

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plu names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled (Insert Title) SEMICONDUCTOR DEVICE AVOIDING MALFUNCTION CAUSED BY ILLEGAL INPUT

the specification of which

(Check one of blocks 1, 2 or 3. See note A on back of this page)

1. ☒ is attached hereto.
2. ☐ was filed on _____ as International PCT Application Serial No. _____ and was amended on _____ (if applicable)
3. ☐ was filed on _____ as U.S. Application Serial No. _____ and was amended on _____ (if applicable)

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I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing d before that of the application for which priority is claimed:

(List prior foreign applications. See note B on back of this page)				Priority Claimed
	Pat. Appln. No.8-334273 (Number)	Japan (Country)	13/December/1996 (Day/Month/Year Filed)	☒ Yes ☐ No
	(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No
	(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No
	(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No

(See Note C on back of this page) ☐ See attached list for additional prior foreign applications

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or PCT Internation application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of th application is not disclosed in the prior application(s) in the manner provided by the first paragraph of Title 35, United States Cod §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) whi occurred between the filing date of the prior application and the national or PCT International filing date of this application:

(List prior U.S. Applications or PCT International applications designating the U.S.)			
	(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
	(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

12 And I hereby appoint as principal attorneys David T. Nikaido, Reg. No. 22,663; Charles M. Marmelstein, Reg. No. 25,895; Geor E. Quam, Jr., Reg. No. 27,931; Robert B. Murray, Reg. No. 22,980; Steven S. Postman, Reg. No. 18,570; B. Marcie Emas, Re No. 32,131; Michael G. Gilman, Reg. No. 19,114, Douglas H. Goldhush, Reg. No. 33,125; Kevin C. Brown, Reg. No. 32,46 Monica Chin Kitts, Reg. No. 36,105; Sharon N. Kleiner, Reg. No. 36,335, and John R. Pusz, Reg. No. 37,327.

Please direct all communications to the following address: NIKAIDO, MARMELSTEIN, MURRAY & ORAM
Metropolitan Square
655 Fifteenth Street, N.W., Suite 330 - G Street Lobby
Washington, D.C. 20005-5701
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and beli are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so mac are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful fal statements may jeopardize the validity of the application or any patent issued thereon.

(See Note D on back of this page)

Full name of sole or first inventor Naoharu Shinozaki

Inventor's signature Naoharu Shinozaki May 16, 1997 (Date)

Residence Kawasaki-shi, Kanagawa, Japan

Citizenship Japan

Post Office Address c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211 Japan

08229880 08/22/97

EXHIBIT
tabbies V

US006104486A

United States Patent [19]

Arimoto

[11] Patent Number: 6,104,486

[45] Date of Patent: *Aug. 15, 2000

[54] **FABRICATION PROCESS OF A SEMICONDUCTOR DEVICE USING ELLIPSOMETRY**

[75] Inventor: Hiroshi Arimoto, Kawasaki, Japan

[73] Assignee: Fujitsu Limited, Kawasaki, Japan

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: 08/774,272

[22] Filed: Dec. 27, 1996

[30] Foreign Application Priority Data

Dec. 28, 1995 [JP] Japan 7-343924

[51] Int. Cl.[7] G01J 3/00

[52] U.S. Cl. 356/300; 356/305; 356/310; 356/322; 356/337; 356/340; 356/345; 356/351; 356/364; 356/128; 250/492.1; 250/492.2; 250/492.22; 250/492.3

[58] Field of Search 356/300, 305, 356/310, 322, 337, 340, 345, 351, 364, 128; 250/492.1, 492.2, 492.22, 492.3

[56] References Cited

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FOREIGN PATENT DOCUMENTS

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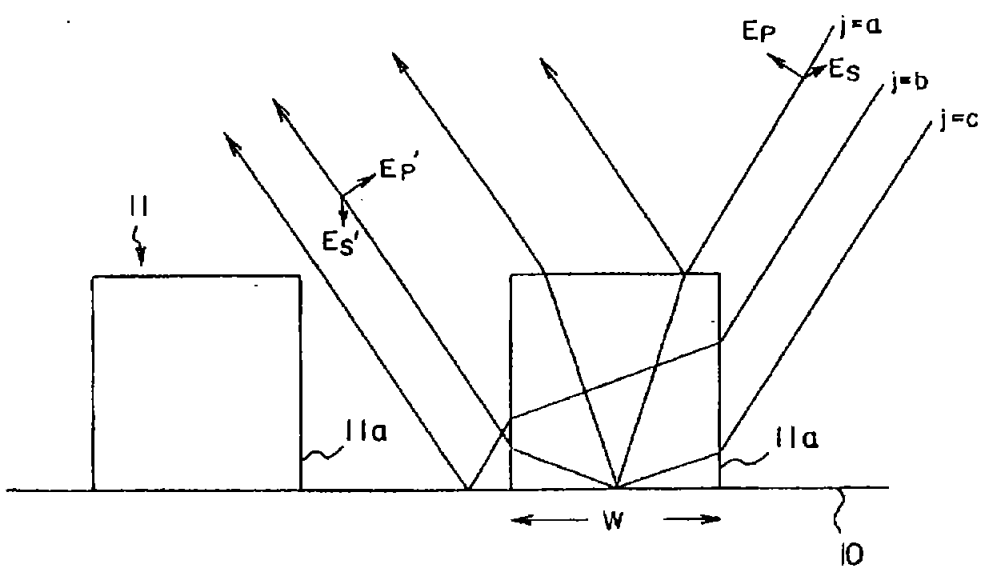
"Ultraviolet–visible ellipsometry for process control during the etching of submicrometer features", N. Blayo et al., AT&T Bell Laboratories, Murray Hill, New Jersey (Sep. 28, 1994); Optical Society of America, vol. 12, No. 3/Mar. 1995, pp. 591–599.

Primary Examiner—Christopher L. Chin
Assistant Examiner—Bao-Thuy L. Nguyen
Attorney, Agent, or Firm—Armstrong, Westerman, Hattori, McLeland & Naughton

[57] **ABSTRACT**

A method of fabricating a semiconductor device includes the steps of illuminating a structure formed on a surface of a substrate by an incident optical beam incident to the structure with a predetermined incident angle with respect to the surface, measuring a polarization state of an exiting optical beam exiting from the structure in response to an illumination of the structure by the incident optical beam, and evaluating a size of the structure in a direction parallel to the surface from the polarization state of the exiting optical beam, and adjusting a parameter of production of a semiconductor device in response to the size.

11 Claims, 24 Drawing Sheets



US006292428B1

(12) **United States Patent**
Tomita et al.

(10) **Patent No.: US 6,292,428 B1**
(45) **Date of Patent: Sep. 18, 2001**

(54) **SEMICONDUCTOR DEVICE RECONCILING DIFFERENT TIMING SIGNALS**

(75) Inventors: **Hiroyoshi Tomita; Tatsuya Kanda,** both of Kawasaki (JP)

(73) Assignee: **Fujitsu Limited,** Kanagawa (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/240,007**

(22) Filed: **Jan. 29, 1999**

(30) **Foreign Application Priority Data**

Feb. 3, 1998 (JP) 10-022257

(51) **Int. Cl.**[7] **G11C 8/00**
(52) **U.S. Cl.** 365/233; 365/230.08; 365/189.05
(58) **Field of Search** 365/233, 230.08, 365/189.05, 240

(56) **References Cited**

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6,064,625		5/2000	Tomita .	

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10-269781	10/1998	(JP) .
11-16346	1/1999	(JP) .
12-163954	6/2000	(JP) .
12-40363	8/2000	(JP) .

OTHER PUBLICATIONS

Korean Intellectual Property Office Action Translation, dated Dec. 6, 2000, 2 Pages with Japanese Unexamined Patent Publication No. Hei 7-141870 (Jun. 2, 1995), 1 Page.

* cited by examiner

Primary Examiner—Huan Hoang
(74) *Attorney, Agent, or Firm*—Arent Fox Kintner Plotkin & Kahn, PLLC

(57) **ABSTRACT**

A semiconductor device which receives addresses in synchronism with a clock signal and receives data in synchronism with a strobe signal includes address-latch circuits, a first control circuit which selects one of the address-latch circuits in sequence in response to the clock signal, and controls the selected one of the address-latch circuits to latch a corresponding one of the addresses in response to the clock signal, and a second control circuit which selects one of the address-latch circuits in sequence in response to the strobe signal, and controls the selected one of the address-latch circuits to output a corresponding one of the addresses in response to the strobe signal.

42 Claims, 25 Drawing Sheets

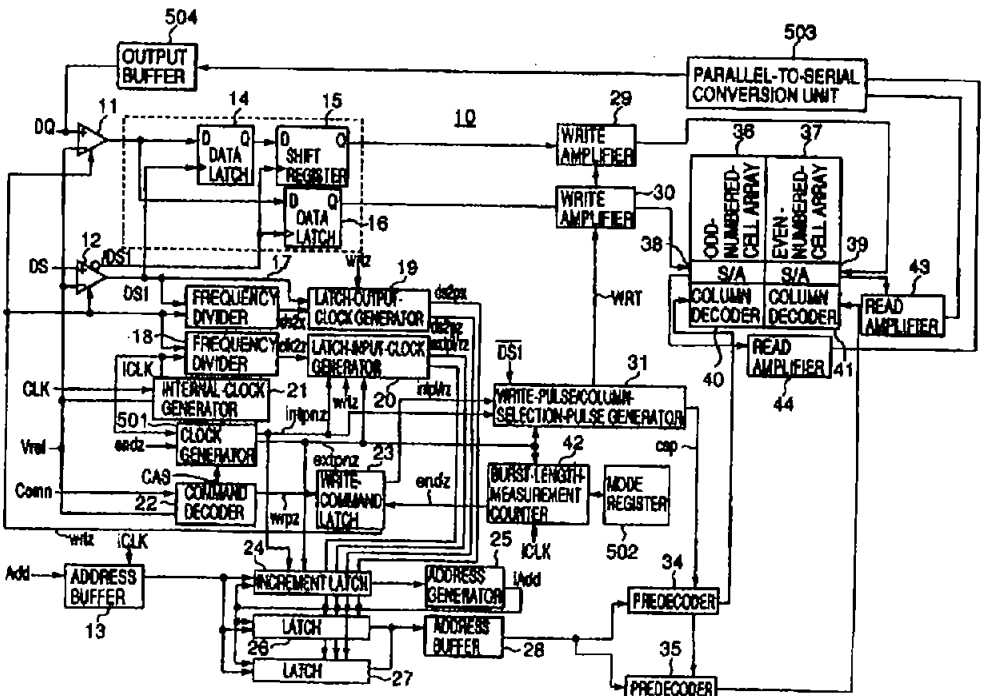

EXHIBIT X

N, M, M & O Docket No. ________

NIKAIDO, MARMELSTEIN, MURRAY & ORAM LLP

Declaration For U.S. Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled (Insert Title) SEMICONDUCTOR DEVICE RECONCILING DIFFERENT TIMING SIGNALS

the specification of which

(Check one of blocks 1, 2 or 3. See note A on back of this page)

1. ☒ is attached hereto.
2. ☐ was filed on ________ International PCT Application Serial No. ________ as and was amended on ________ (if applicable)
3. ☐ was filed on ________ U.S. Application Serial No. ________ as and was amended on ________ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application for which priority is claimed:

(List prior foreign applications. See note B on back of this page)

(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
Pat. Appln. No.10-022257	Japan	3/February/1998	☒ Yes ☐ No
			☐ Yes ☐ No
			☐ Yes ☐ No

(See Note C on back of this page) ☐ See attached list for additional prior foreign applications

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(List prior U.S. Applications)

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

And I hereby appoint as principal attorneys David T. Nikaido, Reg. No. 22,663; Charles M. Marmelstein, Reg. No. 25,895; George E. Oram, Jr., Reg. No. 27,931; Robert B. Murray, Reg. No. 22,980; Martin S. Postman, Reg. No. 18,570; E. Marcie Emas, Reg. No. 32,131; Douglas H. Goldhush, Reg. No. 33,125; Kevin C. Brown, Reg. No. 32,402; Monica Chin Kitts, Reg. No. 36,105; Sharon N. Klesner, Reg. No. 36,335 and Richard J. Berman, Reg. No. 39,107.

Please direct all communications to the following address: NIKAIDO, MARMELSTEIN, MURRAY & ORAM LLP
Metropolitan Square
655 Fifteenth Street, N.W., Suite 330 - G Street Lobby
Washington, D.C. 20005-5701
(202) 638-5000 Fax: (202) 638-4810

EXHIBIT Y

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

(See Note D on back of this page)

Full name of sole or first inventor Hiroyoshi Tomita

Inventor's signature *Hiroyoshi Tomita* Jan. 25, 1999 Date

Residence Kawasaki-shi, Kanagawa, Japan

Citizenship Japan

Full name of second joint inve if any Tatsuya Kanda

Inventor's signature Tatsuya Kanda Jan. 25, 1999

Residence Kawasaki-shi, Kanagawa, Japan Date

Citizenship Japan

Post Office Address c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211-8588 Japan

Full name of third joint inventor, if any

Inventor's signature Date

Residence

Citizenship

Post Office Address

Full name of fourth joint inventor, if any

Inventor's signature Date

Residence

Citizenship

Post Office Address

Full name of fifth joint inventor, if any

Inventor's signature Date

Residence

Citizenship

Post Office Address

Full name of sixth joint inventor, if any

Inventor's signature Date

Residence

Citizenship

Post Office Address

Full name of seventh joint inventor, if any

Inventor's signature Date

Residence

Citizenship

Post Office Address

Full name of eighth joint inventor, if any

Inventor's signature Date

Residence

Citizenship

Post Office Address

Full name of ninth joint inventor, if any

Inventor's signature Date

Residence

Citizenship

Post Office Address

US006320819B2

(12) **United States Patent**
Tomita et al.

(10) **Patent No.: US 6,320,819 B2**
(45) **Date of Patent: Nov. 20, 2001**

(54) **SEMICONDUCTOR DEVICE RECONCILING DIFFERENT TIMING SIGNALS**

(75) Inventors: **Hiroyoshi Tomita; Tatsuya Kanda,** both of Kawasaki (JP)

(73) Assignee: **Fujitsu Limited, Kawasaki (JP)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/733,961**

(22) Filed: **Dec. 12, 2000**

Related U.S. Application Data

(62) Division of application No. 09/240,007, filed on Jan. 29, 1999.

(30) **Foreign Application Priority Data**

Feb. 3, 1998 (JP) 10-022257

(51) **Int. Cl.**[7] **G11C 8/00**

(52) **U.S. Cl.** 365/233; 365/189.05; 365/230.08; 365/194

(58) **Field of Search** 365/233, 189.05, 365/230.08, 194

(56) **References Cited**

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6,064,625	5/2000	Tomita .	

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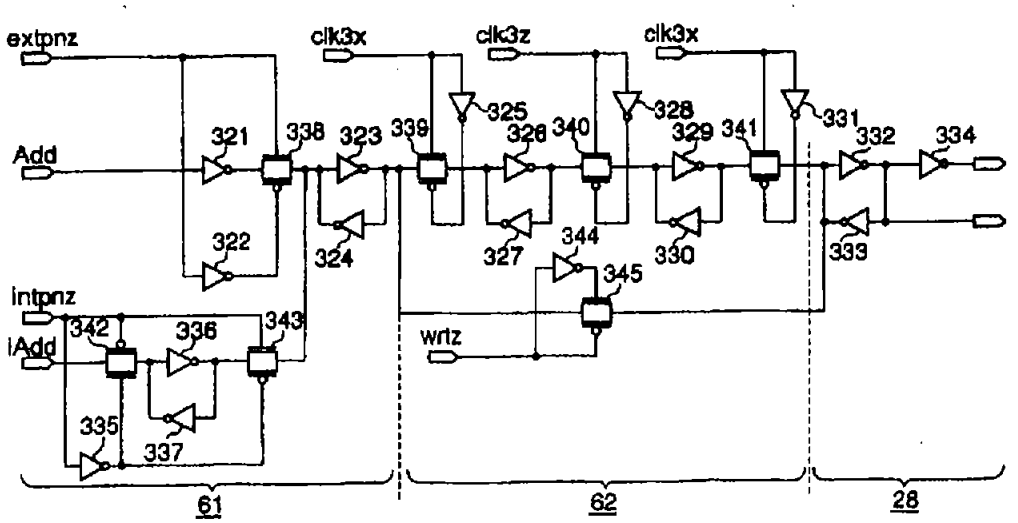
Primary Examiner—Huan Hoang
(74) *Attorney, Agent, or Firm*—Arent Fox Kintner Plotkin & Kahn PLLC

(57) **ABSTRACT**

A semiconductor device which receives addresses in synchronism with a clock signal and receives data in synchronism with a strobe signal includes address-latch circuits, a first control circuit which selects one of the address-latch circuits in sequence in response to the clock signal, and controls the selected one of the address-latch circuits to latch a corresponding one of the addresses in response to the clock signal, and a second control circuit which selects one of the address-latch circuits in sequence in response to the strobe signal, and controls the selected one of the address-latch circuits to output a corresponding one of the addresses in response to the strobe signal.

6 Claims, 25 Drawing Sheets



N, M, M & O Docket No. ___ NIKAIDO, MARMELSTEIN, MURRAY & ORAM LLP

Declaration For U.S. Patent Application

As a below named inventor, I hereby declare that:

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I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled (Insert Title) SEMICONDUCTOR DEVICE RECONCILING DIFFERENT TIMING SIGNALS

the specification of which

(Check one of blocks 1, 2 or 3. See note A on back of this page)

1. ☒ is attached hereto.
2. ☐ was filed on _____ as International PCT Application Serial No. _____ and was amended on _____ (if applicable)
3. ☐ was filed on _____ as U.S. Application Serial No. _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

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				☐ Yes ☐ No
				☐ Yes ☐ No

(See Note C on back of this page) ☐ See attached list for additional prior foreign applications

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(List prior U.S. Applications)	(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
	(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

And I hereby appoint as principal attorneys David T. Nikaido, Reg. No. 22,663; Charles M. Marmelstein, Reg. No. 25,895; George B. Oram, Jr., Reg. No. 27,931; Robert D. Murray, Reg. No. 22,980; Martin S. Postman, Reg. No. 18,570; E. Marcie Emas, Reg. No. 32,131; Douglas H. Goldhush, Reg. No. 33,125; Kevin C. Brown, Reg. No. 32,402; Monica Chin Kitts, Reg. No. 36,105; Sharon N. Kleiner, Reg. No. 36,335 and Richard J. Berman, Reg. No. 39,107.

Please direct all communications to the following address:

NIKAIDO, MARMELSTEIN, MURRAY & ORAM LLP
Metropolitan Square
655 Fifteenth Street, N.W., Suite 330 - G Street Lobby
Washington, D.C. 20005-5701
(202) 638-5000 Fax: (202) 638-4810

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

(See Note D on back of this page)

Full name of sole or first inventor Hiroyoshi Tomita

Inventor's signature Hiroyoshi Tomita Jan. 25, 1999

Residence Kawasaki-shi, Kanagawa, Japan Date

Citizenship Japan

Post Office Address c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211-8588 Japan

EXHIBIT AA

Full name of second joint inventor, if any Tatsuya Kanda

Inventor's signature Tatsuya Kanda Date Jan. 25, 1999

Residence Kawasaki-shi, Kanagawa, Japan

Citizenship Japan

Post Office Address c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211-8588 Japan

Full name of third joint inventor, if any

Inventor's signature Date

Residence

Citizenship

Post Office Address

Full name of fourth joint inventor, if any

Inventor's signature Date

Residence

Citizenship

Post Office Address

Full name of fifth joint inventor, if any

Inventor's signature Date

Residence

Citizenship

Post Office Address

Full name of sixth joint inventor, if any

Inventor's signature Date

Residence

Citizenship

Post Office Address

Full name of seventh joint inventor, if any

Inventor's signature Date

Residence

Citizenship

Post Office Address

Full name of eighth joint inventor, if any

Inventor's signature Date

Residence

Citizenship

Post Office Address

Full name of ninth joint inventor, if any

Inventor's signature Date

Residence

Citizenship

Post Office Address

TEKER TORRES & TEKER, P.C.
130 Aspinall Ave., Suite 2A
Hagåtña, Guam 96910
(671) 477-9891 Telephone
(671) 472-2601 Facsimile

UNPINGCO & ASSOCIATES, LLC
Sinajana Mall, Suite 12B
Sinajana, Guam
(671) 475-8545 Telephone
(671) 475-8550 Facsimile

SHORE CHAN BRAGALONE LLP
325 N. St. Paul Street, Suite 4450
Dallas, Texas 75201
(214) 593-9110 Telephone
(214) 593-9111 Facsimile

Attorneys for Plaintiffs Nanya Technology Corp. and Nanya Technology Corp. U.S.A.

UNITED STATES DISTRICT COURT

DISTRICT OF GUAM

NANYA TECHNOLOGY CORP. and NANYA TECHNOLOGY CORP. U.S.A., *Plaintiffs,* v. FUJITSU LIMITED and FUJITSU MICROELECTRONICS AMERICA, INC., *Defendants.*	Case No. CV-06-00025 **CERTIFICATE OF SERVICE**

I, JOSEPH C. RAZZANO, Esq., hereby declare as follows:

1. I am over the age of majority and am competent to testify regarding the matters stated herein.

2. I hereby certify that on May 3, 2007, a true and exact copy of PLAINTIFFS' RESPONSE TO DEFENDANTS' MOTION TO IMMEDIATELY TRANSFER FOR CONVEN-

IENCE was served via hand delivery on Defendant Fujitsu, Ltd. through its attorneys of record, Calvo & Clark, at their offices located at 655 South Marine Corp. Drive, Tamuning, Guam 96913.

3. I declare under penalty of perjury that the foregoing is true and correct.

DATED at Sinajana, Guam on May 3, 2007.

JOSEPH C. RAZZANO, ESQ.